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09/998,830	12/03/2001	Taiyuu Miyamoto	027260-504	7164

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EXAMINER	
PETRANEK, JACOB ANDREW	
ART UNIT	PAPER NUMBER
2183	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	09/998,830	MIYAMOTO, TAIYUU	
	Examiner	Art Unit	
	JACOB PETRANEK	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,5,6,8 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5,6,8 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-2, 5-6, and 8-9 are pending.

2. The office acknowledges the following papers:

Claims and arguments filed on 12/26/2007.

New Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1-2, 5-6, and 8-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Claims 1 and 5 recite "a first mode, wherein the central processing unit fetches instruction from an external memory, and a second mode, wherein the central processing unit fetches instructions from the internal memory and inhibits fetching instructions from the external memory." Applicant cited pages 7-14 of the specification for support of the claimed limitation. However, the examiner has performed a cursory search of these pages and has found no support of the claimed limitation to show one of ordinary skill in the art that the limitation had possession of the claimed invention at the time the application was filed.

Claim 6 recites "When a first predetermined value is set into the specified area as the limiting code, the central processing unit is configured to fetch instructions from an external memory, and when a second predetermined value is set into the specified area as the limiting code, the central processing unit is configured to fetch instructions from said internal memory and inhibit fetching instructions from said external memory." Applicant cited pages 7-14 of the specification for support of the claimed limitation. However, the examiner has performed a cursory search of these pages and has found no support of the claimed limitation to show one of ordinary skill in the art that the limitation had possession of the claimed invention at the time the application was filed.

5. Claims 2 and 8-9 are rejected due to their dependency.

New Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1-2, 6, and 8-9 are rejected under 35 U.S.C. §103(a) as being unpatentable over Sibigtroth et al. (U.S. 5,432,950).

8. As per claim 1:

Sibigtroth disclosed a microcomputer comprising an internal memory (Sibigtroth: Figure 1 elements 13 and 20)(These elements are the internal memory of the data processing system.), a central processing unit (Sibigtroth: Figure 1 element 14), and a

functional block comprising a peripheral block (Sibigtroth: Figure 1 element 12), built-in said microcomputer, wherein said internal memory has a reprogrammable nonvolatile memory storing user data (Sibigtroth: Figure 1 element 20, column 4 lines 61-67 continued to column 5 lines 1-6)(Official Notice is given that the reconfigurable nonvolatile memories are well known in the art to store multiple types and instances of important data that needs to be saved even after power is removed from the system. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to store additional user data in a reprogrammable nonvolatile memory.), and in which a lock code is written in a specified area (Sibigtroth: Figure 1 element 20, column 4 lines 61-67 continued to column 5 lines 1-6)(The enable signal is stored within element 20.); and

the microcomputer has a first mode, wherein the central processing unit fetches instruction from an external memory, and a second mode, wherein the central processing unit fetches instructions from the internal memory and inhibits fetching instructions from the external memory (Sibigtroth: Figure 1 elements 18, 22, and 24, column 4 lines 15-39 and column 9 lines 36-65)(The second mode is the secure mode and the first mode is the non-secure mode. The second secure mode prohibits fetching instructions from external memory. Figure 1 shows that the processor normally fetches instructions and data via an address bus to the internal and external memories. Therefore, the non-secure mode is capable of fetching instructions from internal and external memory. The secure mode is limited to fetching instructions from internal memory.), and comprising:

a first decoding circuit connected with said nonvolatile memory, which reads out said lock code, and decodes said lock code (Sibigtroth: Figure 2 element 50)(The inverter reads out the enable signal and decodes it.);

a logic circuit that performs a predetermined operation on an externally input mode bit, by the output from the first decoding circuit (Sibigtroth: Figure 2 element 52)(The AND gate takes in the decoded enable bit and the instruction fetch bit, which is external to all circuits shown in figure 1, including the instruction inhibit unit.); and

a second decoding circuit that decodes the processed mode bit by receiving the output from said logic circuit, and sends the obtained results to said functional block (Sibigtroth: Figure 2 element 54)(The OR circuit is the second decoding circuit, which decodes the bit output from the AND circuit, and sends its output to the functional block.), wherein

when a predetermined value is set into the specified area as the lock code, the microcomputer is configured to be set into the second mode (Sibigtroth: Figure 1 element 18, column 9 lines 36-65)(The enable signal indicates the data processing system is in a secure mode. The secure mode inhibits fetching instructions from external memory.).

9. As per claim 2:

Sibigtroth and Phillips disclosed the microcomputer of claim 1, wherein said logic circuit consists of an AND circuit (Sibigtroth: Figure 2 element 52).

10. As per claim 6:

Sibigtroth disclosed a microcomputer comprising internal memory (Sibigtroth:

Figure 1 elements 13 and 20)(These elements are the internal memory of the data processing system.), a central processing unit (Sibigtroth: Figure 1 element 14), and a functional block comprising a peripheral block (Sibigtroth: Figure 1 element 12), built-in said microcomputer, wherein said internal memory comprises a reprogrammable nonvolatile memory storing user data (Sibigtroth: Figure 1 element 20, column 4 lines 61-67 continued to column 5 lines 1-6)(Official Notice is given that the reconfigurable nonvolatile memories are well known in the art to store multiple types and instances of important data that needs to be saved even after power is removed from the system. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to store additional user data in a reprogrammable nonvolatile memory.), and in which a limiting code for limiting a command a memory is written in a specified area (Sibigtroth: Figure 1 element 20, column 4 lines 61-67 continued to column 5 lines 1-6)(The enable signal provides the lock to a specified area.); and said microcomputer comprises:

a first decoding circuit connected with said nonvolatile memory, which reads out said limiting code, and decodes this code (Sibigtroth: Figure 2 element 50)(The inverter reads out the enable signal and decodes it.); and

a second decoding circuit that limits a command to be used, by the output from said first decoding circuit (Sibigtroth: Figure 2 element 54)(The OR circuit is the second decoding circuit, which decodes the bit output from the AND circuit, and sends its output to the functional block.), wherein

when a first predetermined value is set into the specified area as the limiting

code, the central processing unit is configured to fetch instructions from an external memory (Sibigtroth: Figure 1 elements 18, 22, and 24, column 4 lines 15-39 and column 9 lines 36-65)(The enable signal being cleared is the first predetermined value that is stored in element 20. Figure 1 shows that the processor normally fetches instructions and data via an address bus to the internal and external memories. Therefore, the first predetermined value indicating a non-secure mode is capable of fetching instructions from internal and external memory.), and

when a second predetermined value is set into the specified area as the limiting code, the central processing unit is configured to fetch instructions from said internal memory and inhibit fetching instructions from said external memory (Sibigtroth: Figure 1 elements 18, 22, and 24, column 4 lines 15-39 and column 9 lines 36-65)(The enable signal being set is the second predetermined value that is stored in element 20. The second predetermined value that indicates a secure mode prohibits fetching instructions from external memory. Therefore, the second predetermined value indicating a secure mode is limited to fetching instructions from internal memory.).

11. As per claim 8:

Sibigtroth disclosed the microcomputer of claim 1, wherein said reprogrammable memory consists of a data memory and a program memory (Sibigtroth: Figure 1 element 13, column 4 lines 3-8)(Memory 13, a portion of the memory from claim 1, contains both instructions, data, and is reprogrammable.).

Sibigtroth failed to teach non-volatile memory.

However, Official Notice is given that designing memories as non-volatile allows

data and instructions to remain on the disk when the power is removed, and it is well known in the art to design memories as non-volatile for this purpose. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to design the memory 13 as non-volatile since Official Notice is given that it is well known to design memories as non-volatile memories so that they can retain data when their power is removed. This would cause the entire memory (memory 13 and Programmable Security Device 20) to be reprogrammable and nonvolatile, and to contain both data and instructions.

12. As per claim 8:

Sibigtroth disclosed the microcomputer of claim 1, wherein said reprogrammable nonvolatile memory consists of a data memory and a program memory. (From another point of view than the above rejection of claim 8, While Programmable Security Device is both reprogrammable and nonvolatile (column 4, line 61 to column 5, line 32), it alone does not contain both data and instructions.)

However, Sibigtroth suggests the any memory device may be used for Programmable Security Device 20. Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to integrate the Programmable Security Device 20 with the Memory 13 since it has been held use of one piece construction instead of the reference structure is matter of obvious engineering choice (In re Larson, 340 F.2d 965, 967, 144 USPQ 347, 349 (CCPA 1965)., and In re Wolfe, 251 F.2d 854, 855, 1 16, USPQ 443, 444 (CCPA 1958)) and since Sibigtroth suggests that any memory device can be used to as the Programmable Security Device 20.

Integrating the memories would cause there to be one reconfigurable, non-volatile memory that contains both the lock code (data) and other data and instructions.

13. As per claim 9:

Sibigtroth disclosed the microcomputer of claim 1, wherein the logic circuit masks the input mode bit by the decoded lock code (Sibigtroth: Figure 2 element 52)(The selector circuit (And gate 52) takes decoded enable bit and Instruction Fetch bit, and based on the output of the AND gate 52, the external terminal (shown in figure 2) performs different functions, i.e., either allowing the bus 30 to connect to the Data bus 24 or not allowing. The AND circuit provides the mask.).

14. Claim 5 is rejected under 35 U.S.C. §103(a) as being unpatentable over Sibigtroth et al. (U.S. 5,432,950), in view of Phillips et al. (U.S. 6,505,279).

15. As per claim 5:

Sibigtroth disclosed a microcomputer comprising an internal memory (Sibigtroth: Figure 1 elements 13 and 20)(These elements are the internal memory of the data processing system.), a central processing unit (Sibigtroth: Figure 1 element 14), a functional block comprising a peripheral block, built-in said microcomputer, and an external terminal (Sibigtroth: Figure 1 elements 12 and 18)(Element 18 receives external signals on external terminals), wherein said internal memory comprises a reprogrammable nonvolatile memory storing user data (Sibigtroth: Figure 1 element 20, column 4 lines 61-67 continued to column 5 lines 1-6)(Official Notice is given that the reconfigurable nonvolatile memories are well known in the art to store multiple types

and instances of important data that needs to be saved even after power is removed from the system. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to store additional user data in a reprogrammable nonvolatile memory.), and in which a function-selecting code for selecting the function of the external terminal is written in a specified area (Sibigtroth: Figure 1 element 20, column 4 lines 61-67 continued to column 5 lines 1-6)(The enable signal is stored within element 20 and is used for selecting a function of the external terminal connecting to elements 18 and 12); and said microcomputer comprises:

a first decoding circuit connected with the nonvolatile memory, which reads out said function-selecting code and decodes this code (Sibigtroth: Figure 2 element 50)(The inverter reads out the enable signal and decodes it.); and

a selector circuit that selects a function of the external terminal by receiving the output from said first decoding circuit (Sibigtroth: Figure 2 element 52, column 4 lines 61-67 continued to column 5 lines 1-32)(The selector circuit (And gate 52) takes decoded enable bit and Instruction Fetch bit, and based on the output of the AND gate 52, the external terminal (shown in figure 2) performs different functions, i.e., either allowing the bus 30 to connect to the Data bus 24 or not allowing.), wherein

the function-selecting code comprises a priority over data received via said external terminal to cause an operation mode of the microcomputer to be changed from a first function mode to a second function mode (Sibigtroth: Figure 2 element 50, column 4 lines 32-39 and lines 61-67 continued to column 5 lines 1-6)(The enable signal takes priority over the instruction fetch bit for accessing memory. When the

enable signal is active, the operation mode changes to secure mode, which is a second function mode.), wherein in the first function mode the central processing unit is configured to fetch instructions from an external memory, and in the second function mode the central processing unit is configured to fetch instructions from the internal memory and inhibit fetching instructions from said external memory (Sibigtroth: Figure 1 elements 18, 22, and 24, column 4 lines 15-39 and column 9 lines 36-65)(The second mode is the secure mode and the first mode is the non-secure mode. The second secure mode prohibits fetching instructions from external memory. Figure 1 shows that the processor normally fetches instructions and data via an address bus to the internal and external memories. Therefore, the non-secure mode is capable of fetching instructions from internal and external memory. The secure mode is limited to fetching instructions from internal memory.).

Sibigtroth failed to teach the function-selecting code comprises a plurality of bits.

However, Phillips disclosed the function-selecting code comprises a plurality of bits (Phillips: Table 1, column 2 lines 41-67 and column 4 lines 43-63)(The combination results in the security byte of Phillips, which is a lock code for the flash memory of Phillips that is a plurality of bytes and is stored within the flash memory, being stored within element 20 of Sibigtroth.).

The advantage of using the locked byte method of Phillips is that it allows for authorized users to reprogram the memory blocks when needed. The locked byte also offers flexibility in the level of security given to the memory device through a plurality of different byte codes. One of ordinary skill in the art would have been motivated by

these advantages to implement the security byte of Phillips into the programmable security device of Sibigtroth. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the security byte of Phillips into Sibigtroth for the advantage of allowing authorized users to reprogram security measures and allow for a wide range of security levels.

Response to Arguments

16. The arguments presented by Applicant in the response, received on 12/26/2007 are considered persuasive.

17. Applicant argues "Sibigtroth does not teach or suggest that the central processing unit fetches instructions from either the internal memory or the external memory in accordance with the lock code stored in the internal memory, as required by Applicant's claims."

This argument is found to be persuasive for the following reason. The examiner agrees that Sibigtroth failed to teach the claimed limitation. However, due to the amendment, a new ground of rejection has been given.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Guttag (U.S. 4,521,853), teaches disabling a external interface for a secure mode.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JACOB PETRANEK whose telephone number is (571)272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Jacob Petranek
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